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A Modified Design of Test Pattern Generator for Built-In-Self-Test Applications

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ABSTRACT
Test Pattern Generators (TPG) are very important logic part of the Circuits that have self-test features. Nowadays, the self-test feature is an in-built part of the modern application hardware designs. This feature enables the user to test and verify the specific hardware failure with the help of the hardware itself. To enable self-test an extra operational and control circuit is required by the application based operational and control circuit. The size of the self-test block is generally small as compared to the actual hardware. Most of the self-test hardware includes Linear Feedback Shift Register (LFSR) to generate the test signal pattern in the self-test mode of circuit operation. In the present work a simple 3-FF based modified design of TPG is designed and simulated to generate a 4-bit test signal sequence. The present work also shows FPGA based simulation and synthesis of a 16-bit TPG design using the 4-bit TPG. The present TPG design concept can be replicated to generate a test sequence of higher bit length for advanced applications. The present design is simulated on Xilinx tool for functional verification.

Keywords: LFSR, TPG, Xilinx, XOR.

I. INTRODUCTION

Nowadays, a configurable hardware design performance can be evaluated using its operational parameters like speed and power, and also with the reliability of the hardware performance in terms to with-stand against the hardware faults. This has increased the importance of Self-Testing feature in the analysis of circuit performance. The various parts of a modern digital application circuit include processor core(s), memory, external interface circuit, wireless communication hardware, audio-video processing hardware, etc. The overall performance of the design is analyzed by the individual performance of the underlying circuit units. Modern electronic circuit applications are becoming more and more embedded with the software based programs. These programs make it easy to track the performance of individual hardware unit. The availability of configurable hardware with high logic capacity, like FPGA, also allows the implementation of software driven hardware with less time to market. This can be verified by the day-to-day emerging application gadgets in the world market. FPGA has opened the ways of development of complex System-On-Chip designs for technological developments in the electronic application specific circuit design. FPGA allows configuration of millions of gates in a single chip with the help of software programming platform.

The configurable hardware requires very less time to bring an application gadget into the market. This hardware sometime misbehaves due to faulty transistor or hardware component. So the designs are implemented with a feature to test the occurrence of fault in the behavior of the hardware unit. These self-testing logic designs perform only when the hardware is not performing its regular function. The self-testing activity requires a sequence of random pattern to give to the hardware unit that is under test. The self-testing circuit compares the functional performance of the hardware under test with the desired performance output of the hardware under test. The hardware unit is tested for multiple random inputs so that each of the internal components of that unit should be involved in the functional activity for the generation of the output. Thus the hardware generated output has the effect of probably all the hardware components. A number of random inputs processed by the hardware cover most of the functional states that can verify the authenticity of hardware performance. Fig 1 shows the basic architecture of a Self-Test circuit model.

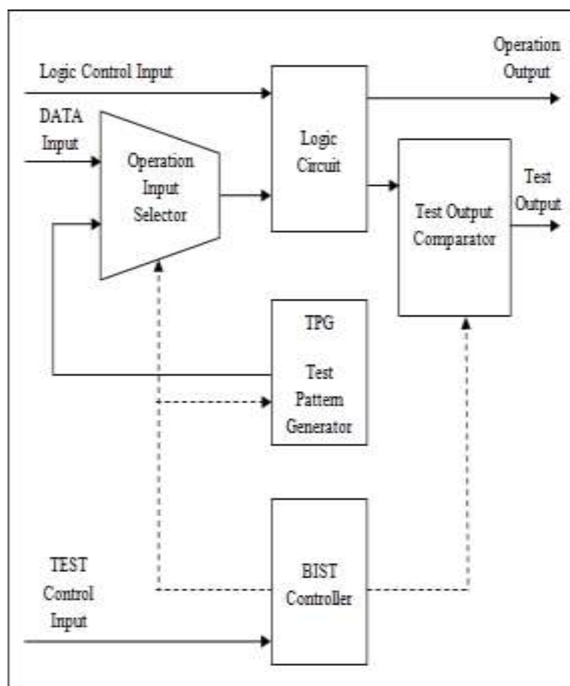

Fig. 1 RTL Block Diagram of Proposed 4-bit Test Pattern

The self-testing feature is required in the hardware for self-diagnosis or self-testing. This feature helps the configurable hardware to test itself and to re-locate the hardware resource within the integrated circuit in case of hardware fault. The generation of random sequence is very important in the self-test circuits. In most of the self-test circuits the random sequence has only a few random values so that the testing can be performed with less time and with minimum power consumption. A low power circuit is always desired in the design of such circuits. Random sequence number generation is used in many other applications also such as circuit testing, cryptography, data encryption, computer games, etc. In the present paper a critical consideration is given to a modified design of a random sequence generation with a reduced hardware. The test pattern is generated using a modified architecture by reducing the number of sequential component as compared to the conventional design components. The present paper is organized as follows: Section-II presents the Literature Review on the TPG and its applications. Section-III describes the design of proposed Test Pattern Generator. Section-IV presents simulation and synthesis results. Section-V presents the conclusion drawn on the basis of the performed design. Finally the references are mentioned.

II. Literature Review

Many architectures of test pattern generator are proposed by scholars and researchers in their work regarding parametric advantages like high speed or low power design of BIST based logic circuit for hardware design applications. In [1] a low power TPG design is proposed using a low-power Linear Feedback Shift Register for BIST structures. This design proposes the approach of reducing the switching activity based on single input change pattern generated by a counter and a gray-code converter. Reference [2] proposes an FPGA Implementation of LFSR based Pseudorandom Pattern Generator for MEMS Testing. This design has the characteristic advantages of high speed, low power consumption and it is especially suited in the processors that require uniform distribution random numbers. Reference [3] presents different techniques to modify the BIST architecture to reduce the power consumption by the self-test circuit thereby finding an optimal choice without compromising upon fault coverage. A Low Power linear feedback shift register based low power test pattern generator design is proposed in [4,5]. These designs mainly focus on test vector are generation in the BIST to reduce the power consumption. In this paper the transition is reduced by generating the gray-code. Reference [6] proposes FPGA implementation of 16-bit BBS and LFSR PN Sequence Generator. This paper shows the change in the logic of PN sequence generator by changing the seed in LFSR or by changing key used in BBS. A paper with FPGA based N-bit LFSR to generate random sequence number design is proposed in [7]. This design presents study the performance and analysis of the behavior of randomness in LFSR. A review of LP-TPG using LP-LFSR for Switching Activities is presented in [8, 9, 10]. Reference [8] presents structures of multiplier, LFSR, LP-TPG and BIST. Reference [11] presents a simulation study of TPG using Shift Register based on 16th Degree Primitive Polynomials. This paper focuses on a comparative study of different types of implementations for a LFSR for 16th degree irreducible or primitive polynomials. Pseudo-Random number generation by using WELL and Re-seeding method is presented in [12]. This paper presents a random number generation by using WELL method first and its performance was analyzed. The repeating pattern is avoided by Re-seeding method.

The TPG is the major component of BIST hardware. Many FPGA implementation based BIST application circuits for power and speed optimized designs are proposed and simulated by researchers. A low power structure design of 2D-LFSR and encoding technique for BIST is proposed in [13]. In this paper, the configurable 2-D LFSR test generator can be adopted in two basic BIST options: test-per-clock (parallel BIST) and test-per-scan (serial BIST). Generally, a circuit consumes more power in test mode than in normal mode. This extra power consumption can give rise to severe hazards. The

scheme proposed in this paper takes advantage of the fact that the number of transitions in a test blocks is always less than the number of blocks that do not contain transitions and the logic value fed into the scan chain is simply held constant. This approach reduces the transition count in the scan chains and thus minimizing power consumption.

A research article in presented in [14] that proposes a logic BIST using linear feedback shift register to generate test pattern with low power consumption. This design reduces the number of transitions at the input of test hardware using bit swapping technique. BIST architecture for online input vector monitoring design is proposed in [15]. This paper is based on the concept of monitoring a set of vectors reaching the test hardware inputs at the time of normal operation and the use of a SRAM based memory like architecture that store the relative locations of the vectors that reach the circuit inputs. A novel test pattern generator suitable for BIST structures is presented in [16]. This design uses the characteristic information of the circuit under test to generate the test vectors. This TPG reduces the switching activity among the test patterns to reduce the power and to improve the coverage of faults. Another approach of high fault covering TPG design is presented in [17]. Reference [18] presents an advanced BIST design with Low Power LBIST and BDS oriented March Algorithm implementation for Intra Word Coupling Faults. This paper focuses read faults with classic faults with an improvement in the efficiency of the BIST architecture and test time in detecting the faults. An FPGA prototyping of universal asynchronous receiver transmitter with low power TPG based BIST architecture is proposed in [19]. This paper presents a low power TPG for BIST without affecting the fault coverage. A BIST enabled I^2C protocol hardware implementation on FPGA is presented in [20]. This design proposes a self-test design of a common hardware interface protocol for high speed communication device.

III. PROPOSED DESIGN OF TEST PATTERN GENERATOR

For the implementation of BIST circuit, a test pattern generator with random output value is required. The present work gives a design of a test pattern generator with reduced logic hardware. 4-bit TPG logic is implemented using a gate level architecture. The block diagram of the proposed 4-bit TPG is shown in Fig 2. The proposed design is realized using Xilinx ISE Tool. The RTL Schematic of the proposed 4-bit TPG is shown in Fig 3.

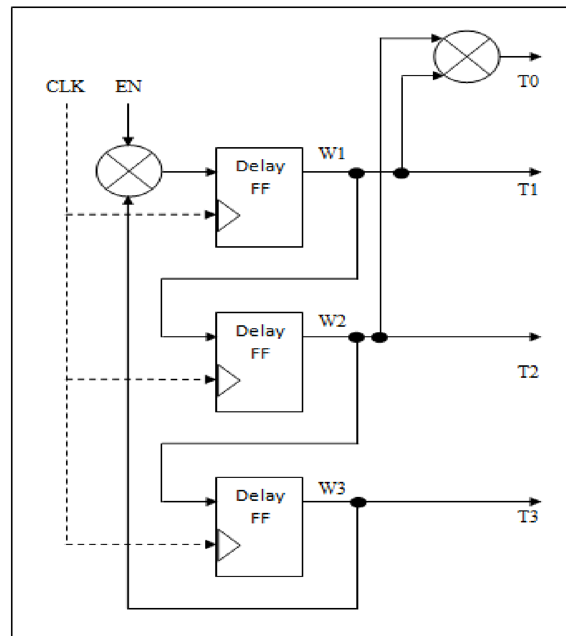

Fig. 2 Block Diagram of Proposed 4-bit Test Pattern Generator

For TPG realization, a modified design of linear-feedback-shift-register (LFSR) is used in this paper. A 3-flipflop based design is used for the generation of a 4-bit random number. It is a comparative small design realization as compared to other existing TPG designs. The conventional TPG have a register-to-bit ratio of ‘1’. In the proposed design, the TPG has a register-to-bit ratio of 3:4, i.e., a 4-bit test pattern output is generated by using 3-flipflops in the generator design. This design uses 3-flipflops with linear feed-back and the output of the last flip-flop is XOR-ed with the control input *Enable* to trigger the random number generation.

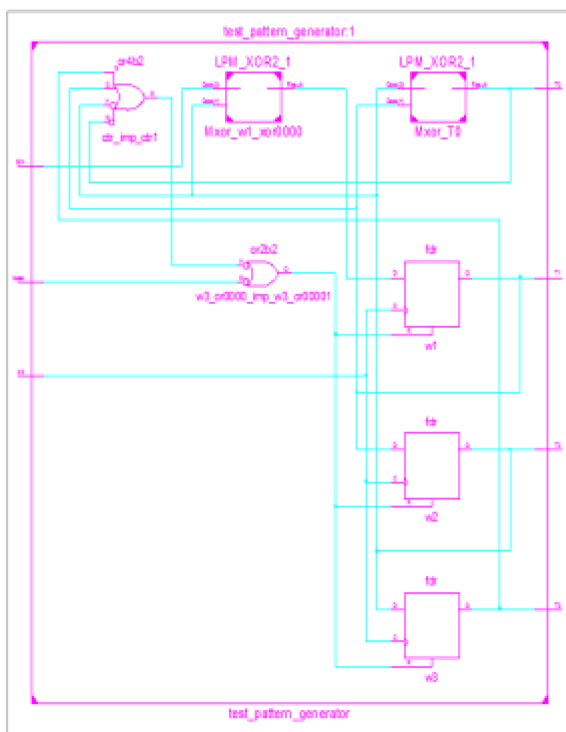

Fig. 3 RTL Schematic of Proposed 4-bit TPG

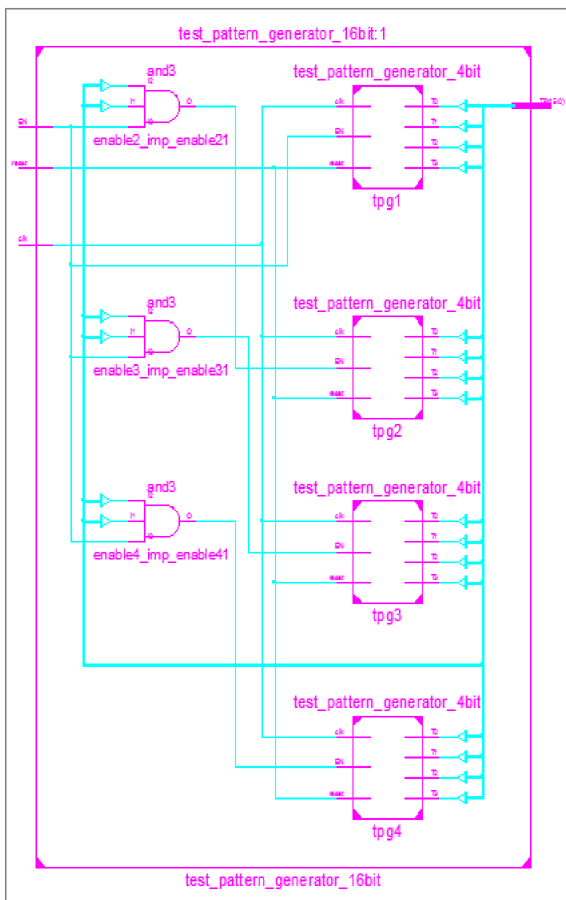

Fig. 4 RTL Schematic of Proposed 16-bit TPG

The outputs of the first two flipflops are XOR-ed to generate the fourth output bit of the TPG. Logic-'0' value on *Enable* input drive the output of the TPG to logic "0000" output. Logic-'1' signal on the *Enable* input activates the hardware to generate random 4-bit signal. The proposed 4-bit design can be used in a combination of multiple blocks to generate a higher-length of random numbers. Fig 4 shows the RTL Schematic of a 16-bit TPG that is designed using four 4-bit proposed TPGs. These four TPGs are connected in series. The Enable input of the TPG is controlled by the output of the previous TPG.

IV. SIMULATION AND SYNTHESIS RESULTS

A modified TPG design in the proposed work is implemented using VHDL Hardware Description Language on Xilinx ISE Tool. The simulation of the design is performed on Xilinx ISim Tool using VHDL Test-Bench. The waveform simulation result of the 4-bit TPG and the 16-bit TPG are shown in Fig 4 and Fig 5 respectively. The proposed design of 4-bit TPG generates four different test pattern of output. When 'N' number of such block are connected in series, as performed in this paper then the total number of different patterns becomes (4^N). Since the proposed 16-bit TPG involves four 4-bit TPG units so it generates 4^4 = 256 different output patterns. The hardware utilization summary of the proposed 4-bit and 16-bit TPG designs are presented in Table 1 and Table 2 respectively. The hardware synthesis is performed on Xilinx Spartan-3E FPGA. An FPGA offers a low power realization of any digital design.

Table 1
Hardware Utilization Summary of 4-bit TPG

Spartan-3E XC3S500E-4PQ208	Total	4-bit TPG	
		Used	%
Slices	4656	3	0
Flipflops	9312	3	0
LUTs	9312	3	0

Table 2
Hardware Utilization Summary of 16-bit TPG

Spartan-3E XC3S500E-4PQ208	Total	16-bit TPG	
		Used	%
Slices	4656	7	0
Flipflops	9312	12	0
LUTs	9312	12	0

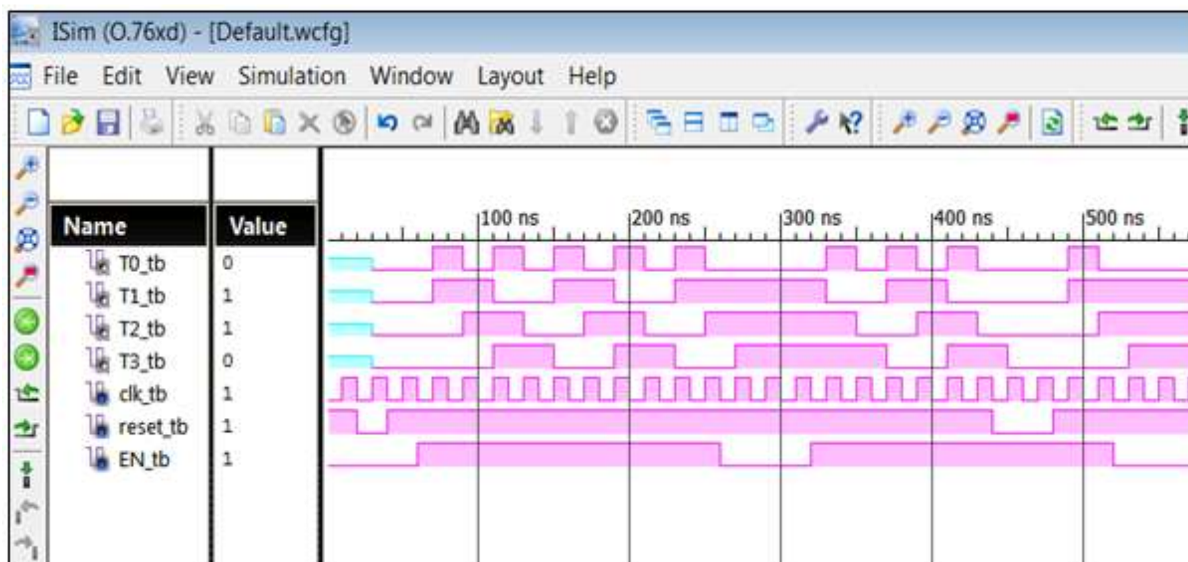

Fig. 3 RTL Schematic of Proposed 4-bit TPG

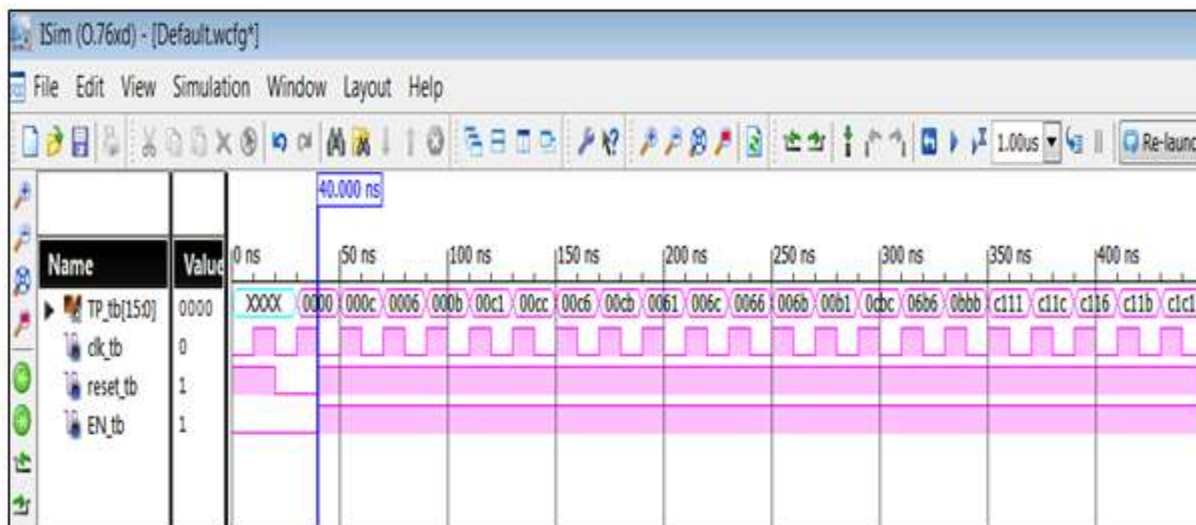

Fig. 4 RTL Schematic of Proposed 16-bit TPG

V. Conclusion

The present work proposes modified design architecture of a test pattern generator. The TPG has a low register-to-bit ratio, i.e., the number of out bits in the generated sequence is more than the number of registers/flipflops in the generator circuit. Thus, with respect to the conventionally proposed designs of TPG it involves less number of registers. This design can be modified by combination of multiple architecture for a long bit sequence generation of random number. In the future work the test pattern generator can be configured to match the application specific requirement of the design for a Built-In-Self-Test based hardware design implementation. The present work also has the scope of combining other existing hardware circuits with this design for a complex logic implementation.

VI. Acknowledgements

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